

(54) METHOD FOR FORMING SOLDER BUMP
 (11) 55-111127 (A) (43) 27.3.1980 (19) JP
 (21) Appl. No. 54-18209 (22) 19.2.1979
 (71) FUJI DENKI SEIZO K.K. (72) MISAO SAGA(1)
 (51) Int. Cl. H01L21 28, B23K1 00

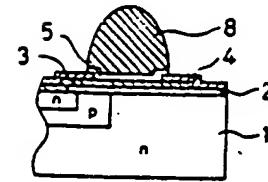
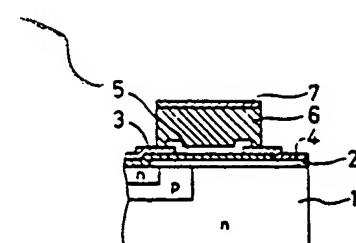
PURPOSE: To form a solder bump which is characterized by the features that a photoresist is readily removed and damages are not remained in characteristic checking, by melting a solder-plated layer at a specified temperature and curing it, thereafter melting the solder layer at a higher temperature and curing it again.

CONSTITUTION: A surface-protecting film 4 is further deposited on an Al wiring 3 which contacts with Si and the window portion of a surface-protecting film 2 on a Si substrate 1, and an underlying metal layer 5 is formed at said window portion. Thereafter, a Pb layer 6 and an Sn layer 7 are stacked by electric plating with a photoresist being a mask. Then, the plated layers 6 and 7 are melted at a temperature less than 320°C, and the photoresist is removed after said layers have been cooled and cured. At this stage, the characteristic check of the element is performed. Thereafter, the temperature is increased again, and the soldering layers are melted again at a temperature higher than the previous melting temperature (e.g., 330~350°C for the solder comprising 90% of Pb and 10% of Sn), thereby a semi-circular solder bump 8 is obtained. In this constitution, even though damages are given in the characteristic check, the remnants of the damages are not remained.

N:

Cu

Ti



⑨ 日本国特許庁 (JP)
⑩ 公開特許公報 (A)

⑪ 特許出願公開
昭55-111127

⑫ Int. Cl.³
H 01 L 21/28
B 23 K 1/00

識別記号

厅内整理番号
7638-5F
6919-4E

⑬ 公開 昭和55年(1980)8月27日
発明の数 1
審査請求 未請求

(全 2 頁)

⑭ はんだバンプ形成方法

⑮ 特 願 昭54-18209

⑯ 出 願 昭54(1979)2月19日

⑰ 発明者 佐賀操

川崎市川崎区田辺新田1番1号
富士電機製造株式会社内

⑮ 発明者 天野彰

川崎市川崎区田辺新田1番1号
富士電機製造株式会社内

⑯ 出願人 富士電機製造株式会社

川崎市川崎区田辺新田1番1号

⑰ 代理人 弁理士 山口巖

明細書

1. 発明の名称 はんだバンプ形成方法

2. 特許請求の範囲

1) はんだりっき層を320℃以下の温度において
加熱して堅固させた後さらに高い温度で再加熱し
て堅固させることを特徴とするはんだバンプ形成
方法。

3. 発明の詳細な説明

本発明はフリップチップ電子などのボンディング
のための電極と接続されるはんだバンプの形
成方法に関する。

このようなはんだバンプを選択加熱により形成
することはバンプ高さの制御が困難で処理コスト
が高い欠点があるので、通常ははんだりっきを利用
して行われる。第1図に示すようにフリップチ
ップ電子においてはシリコン基板1の上に被覆し
た、例えば酸化シリコンから成る表面保護膜2の
表面でシリコンと接続するアルミニウム配線3の
上にさらに、例えば酸化シリコン4から成る表面
保護膜4を被覆し、その間に、例えばTi, Cu,

(1)

NIの3層を順次蒸着して形成する下地金属層5を
被覆する。この下地金属層5の上にホトレジスト
をマスクとしてPb層6およびSn層7を電気めっき
により被覆する。次いでこのPb層6およびSn層7
を340-350℃の温度で融解して合金させ、第2
図に示すような半球状のバンプ8に成形する。
(第2図の第1回と同一の部分には同じ符号が付
してある。)第1回においてPb層の厚さを約50
μm、Sn層の厚さを約10μmにすれば、バンプの合
金は重量比でPb 90%、Sn 10%のはんだとなり、バ
ンプの高さは約100μmとなる。はんだリッキの膜
に被覆したホトレジストは、はんだリッキの直後
に融解すると融点用の有機系の膜がわざと層を剥
離するのでこの融解工程の後で融安される。さら
にははんだに覆われていない下地金属層を融安し、
電子の特性チャックを行う。しかし上述の工程に
おいては電子の特性チャックの間にバンプが損傷
を受けやすい。またはんだ融解時にホトレジスト
が焼付いてその融安が不完全になることがある。

本発明の目的は上述の方法と異なり、ホトレジ

(2)

ストの除去が容易でしかも特性チャートの圖の良
さを残さないはんだバンプの形成方法を提供する
ことにある。

この目的を達成するために本発明に示すく形
方法は次のような工程をとる。すなわち図1に
示すようなはんだかっつきを施した後320°C以下の
温度でカッティング等を施すと、内部接続部のトレリス
トを除去する。この温度ではレジストは實質せず、
現付くことがないので除去は容易である。そして
この段階で電子の特性チャートを行なう。この後再
び温度を上げて前の耐熱温度より高い温度、例えば
Pb 90%、Sn 10%のはんだでは330~350°Cで、
はんだ帶を再熱して図2のような半球状の金
球形状を得る。この再熱段により特性チャートの
間に損傷を受けてもその機能が残ることはなく、
以後の操作に支障を来たすことがない。最後には
んだで覆われない下地金属層をエッチングで除去
した電子は電立工場に付される。

上述の例では、はんだかっつき層はSnかっつきと
Pbかっつきの2層として形成されるが、1層の場合

198255-111127(2)

かっつきにより形成されたはんだかっつき層に対して
も本発明は適用できる。

以上のように本発明によるバンプの形成方法は、
はんだかっつき層の形成を2工程に分けることによ
り、その間にホトレジストの除去や特性チャ
ートの工程等を介在させることができ、得られたバ
ンプが特性的にも外観的にも支障のないものにす
ることを可能にする。

1. 図面の簡単な説明

図1は本発明の適用される例であるアリーブ
ナップ電子の一例分のはんだかっつき後の断面図、
図2は同じくはんだバンプ形成後の断面図である。

1—Pbかっつき層、2—Snかっつき層、3—はんだ
バンプ。

REDACTED 山口 真一

(3)

(4)

Fig. 1

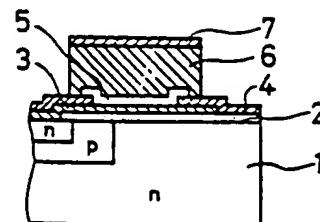
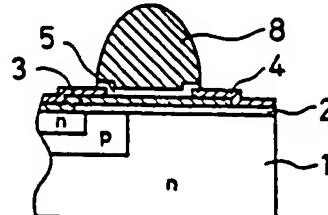


Fig. 2



(19) JAPAN PATENT OFFICE

(12) PUBLIC PATENT REPORT (A)

(11) Patent Number: 55-111127

(43) Opened to Public: Aug. 27, 1980

Office Ref. No.: 7638-5F, 6919-4E

(54) METHOD OF BUILDING SOLDER BUMPS

(72) Inventors: 1. Misao Saga

2. Akira Amano

Fuji Denki Sezo K.K.

Kawasaki-shi, Kawasaki-ku, Tanabe Shinden 1-1

(71) Filed by: Fuji Denki Seizo K.K.

Kawasaki-shi, Kawasaki-ku, Tanabe Shinden 1-1

(21) Appl. No.: 54-18209

(22) Filed on: Feb. 19, 1979

(51) Int. Cl.3 H01L 21/28; B23K 1/00

(74) Legal Representative: Patent Attorney, Iwao Yamaguchi

S P E C I F I C A T I O N S

1. Patent Name:

Method of Building Solder Bumps

2. Field of Patent Application:

A method of building solder bumps by which the solder-plated

layer is first dissolved at a temperature lower than 320°C, then cured, and after that dissolved again at a higher temperature and cured again.

3. Detailed Description

The invention is related to the electroplating method of forming solder bumps, which are used to bring flip-chip elements together.

In general, a weak point of the bumps applied for this purpose so far was the difficulty of controlling the bump height, which consequently increased the processing costs. A solder plating method usually used in bump building is demonstrated in Fig. 1. The elements usually comprising a flip chip are mounted on silicon substrate material (1). The surface-protecting film (2), made of silicon oxide, is covered by aluminum wiring (3). The silicon and the aluminum wiring come into contact at the window section where the surface-protecting film (2) does not cover the silicon substrate. The aluminum wiring is covered by the surface-protecting film made of silicon-(?) film (4), and the window inside the silicon-(?) film (4) is covered by under-bump metallurgy (5) which is composed of three successively deposited layers of Ti, Cu, and Ni. This under-bump metallurgy (5) is masked with a photoresist, and a layer of Pb (6) and a layer of Sn (7) which are laminated by electroplating. Then, the layer of Pb and the layer of Sn are dissolved at a temperature between 340 - 350°C making an alloy. As the result, a semispheric bump (8) is formed, as shown in Fig. 2. (The same numbers are attached to corresponding elements in Fig. 1

and Fig. 2.) If the thickness of Pb layer shown in Fig. 1 is about 50 μm , and if the thickness of Sn layer is about 10 μm , then Pb will make up 90% of the bump-alloy relative weight, and Sn will make up the remaining 10%. The height of the bump will be approximately 100 μm . If the photoresist deposited during the solder plating is removed immediately after the solder plating, the organic acid used for removal will erode the plated layer. For this reason, the photoresist is removed after the dissolving process. After removing the under-bump-metallurgy layer which is not covered by the solder plate, the specific check of the elements is carried out. However, the bumps can easily be damaged when the specific check of elements is carried out. Also, in some cases the photoresist may sinter during the dissolving process, and after that its removal will be incomplete.

The objective of this invention is to produce a result different from the results of the processing described above. This method of solder-bump building provides an easy removal of photoresists and protects from damage during the specific check.

In order to accomplish the objective, this invention introduces a building method as described hereafter. After the solder plating shown in Fig. 1 has been completed, the plated layer is dissolved at a temperature lower than 320°C, and after the cooling and curing the photoresist is removed. The resist does not deteriorate at this temperature, and it can be easily removed because there is no sintering. At this point the specific check is carried out. Then, the temperature is raised above the previous

dissolving temperature which was between 330-350°C for the solder comprised of 90% of Pb and 10% of Sn. Then, the solder layer is dissolved again to build up the final semispheric form, as shown in Fig. 2. Even if a damage occurs when the specific check is carried out, the repeated dissolving process makes sure that the damage does not remain and does not cause problems afterwards. Finally, the under-bump-metallurgy layer which had not been covered by solder is removed by etching, and the flip-chip elements are assembled.

In the above described example, the solder plating was comprised of two layers, the plated Sn and the plated Pb. This invention can also be applied, however, in the solder plating comprised of only one layer of plated alloy.

In summary, this method of building solder bumps divides the dissolving the solder-plated layer into two steps and enables the photoresist removal and the specific check to be carried out between the two steps. The characteristics and the external appearance of the bumps obtained by this method are free of defects.

4. Simple Description of Figures

Fig. 1 shows the cross-sectional view of an application of this invention after the flip-chip elements had been partly solder plated. Fig. 2 shows the same example after the bump form had been built.

6 ... Pb-Plated Layer

7 ... Sn-Plated Layer

8 ... Solder Bump

Legal Representative: Patent Attorney, Iwao Yamaguchi

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- BLACK BORDERS**
- IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- FADED TEXT OR DRAWING**
- BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- SKEWED/SLANTED IMAGES**
- COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- GRAY SCALE DOCUMENTS**
- LINES OR MARKS ON ORIGINAL DOCUMENT**
- REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.